Abstract of the Disclosure:

An integrated memory contains an addressing unit for addressing memory cells for a memory access on the basis of received addressing signals. An addressing calculation logic unit is connected to the addressing unit. The latter can be activated by a test mode signal for a test operation of the memory. The addressing calculation logic unit receives command signals and address signals for the test operation, calculates therefrom the addressing signals for the memory access and feeds the latter into the addressing unit. After an initialization with the loading of initial parameters, the command signals and address signals for the test operation are applied to the addressing calculation logic unit and read/write operations are carried out by an access controller. An integrated memory with implemented BIST hardware, in the case of which a comparatively high functionality and flexibility during the memory test, are nevertheless made possible.

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